EURO-PAR
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TOPIC 4 - HIGH PERFORMANCE ARCHITECTURES AND COMPILERS

CHAIRS

Global Chair
Pedro Petersen Moura Trancoso
Chalmers University of Technology, Gothenburg, Sweden

Local Chair
Matthias Müller
RWTH Aachen, Computer Science, High Performance Computing

Co-Chairs
Angelos Arelakis
ZeroPoint Technologies, Sweden

Alexandra Jimborean
Uppsala University, Sweden

DESCRIPTION

This topic deals with architecture design, languages, and compilation for parallel high performance systems. The areas of interest range from microprocessors to large-scale parallel machines (including multi-/many-core, possibly heterogeneous, architectures); from general-purpose to specialized hardware platforms (e.g., graphic coprocessors, low-power embedded systems); and from architecture design to compiler technology and language design.

On the compilation side, topics of interest include programmer productivity issues, concurrent and/or sequential language aspects, vectorization, program analysis, program transformation, automatic discovery and/or management of parallelism at all levels, autotuning and feedback directed compilation, and the interaction between the compiler and the system at large. On the architecture side, the scope spans system architectures, processor micro-architecture, memory hierarchy, and multi-threading, architectural support for parallelism, and the impact of emerging hardware technologies.

Focus

- Compiling for multi-threaded/multi-core/many-core/vector and heterogeneous processors/architectures
- Compiling for emerging architectures (low-power embedded systems, reconfigurable hardware, processors in memory, coprocessors)
- Iterative, just-in-time, feedback-oriented, dynamic, and machine-learning-based compilation
- Static analysis and interaction between static and dynamic analysis
- Programmer productivity tools and analysis for high-performance architectures
- Program transformation systems
- High level programming models and tools for multi-/many-core and heterogeneous architectures
- Interaction between compiler, runtime system, application, hardware, and operating system
- Parallel computer architecture design – ILP, DLP, multi-threaded, and multi-core processors
- Designs and compiler optimizations for power/performance efficiency
- Software and hardware fault-tolerance techniques
- Memory hierarchy, emerging memory technologies, and 3D stacked memories
- Application-specific, reconfigurable and embedded parallel systems
- Compiler, run-time, and architectural support for dynamic adaptation

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